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A Modified Design for Testability (DFT) Architecture for Power Minimization

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Abstract---In this paper, we propose a novel low power/vitality Outline for-testability (DFT) system in light of circuit apportioning. The objective of the proposed procedure is to minimize the normal power, the crest force and the vitality utilization amid DFT without adjusting the flaw scope. Power dispersal amid output testing is turning into an imperative concern as outline sizes and door densities increment. While a few methodologies have been as of late proposed for diminishing force dissemination amid the movement cycle (least move couldn't care less fill, extraordinary output cells, and sweep chain parceling). This method comprises in dividing the first circuit into two basic subcircuits, so that every subcircuit can be progressively tested through specific trigger strategy. This technique lessens exchanging movement in the circuit-under-test (CUT) and builds the clock recurrence of the checking methodology. An assistant chain is used in this system to keep away from the vast number of moves to the CUT amid the output in procedure. Power prerequisites are generously diminished; additionally, DFT punishments are decreased in light of the fact that no extra multiplexer is used along the output way. Utilizing ISCAS 89 benchmark circuits, this adequacy is to enhance SoC test measures (power, time, and information volume) is tentatively assessed and affirmed.

Index Terms---Circuit-Under-Test (CUT), Design-For-Testability (DFT), Scan Test, Scan Chain Partitioning, Selective Trigger, Shift Cycle.

1. INTRODUCTION

Scan architectures represent an attractive solution for both built-in and external testing of digital integrated circuits (ICs). This is because they increase the controllability and observability of internal nodes of the circuit, are easy to implement, and have relatively low impact on area and performance. A scan-based test cycle has two distinct cycles: shift and capture. Shifting a test pattern into the scan chain occurs simultaneously with shifting out circuit's response to the previous test pattern. In the capture cycle, the test pattern, loaded in the scan chain during the shift cycle, is applied to the circuit under test, and the response of the circuit iscaptured into the scan chain. Rosinger [4] proposed scan chain partitioning reduces shift-power dissipation by a factor of approximately two, without affecting the testing time or the performance of the circuit. Nicolici [5] proposed splits the scan chain into multiple segments based on a compatibility relation between the flip-flops and activates only one segment in each shift clock. An extra test vector, computed using a special ATPG algorithm, is applied during the shift cycle to the primary inputs of the circuit under test in order to further reduce switching due to the shift ripple. A simpler yet very efficient approach first proposed in [6] and extended later in [7], splits the scan chain into length adjusted portions. Apportioning the outline and testing one segment at once has been proposed to diminish dispatch and catch power during built-in self-test (BIST) [8], LOS [9] and LOC [10].

The rest of the paper is organized as follows: Section II illustrates the proposed LOS, LOC, Mixed-at-speed testing, block logic method, and a selective trigger for reduce transition power and prevents redundant switching in combinational logic. Section III presents experimental results in terms of area, delay and power for an ISCAS89 benchmark circuit. Section IV presents related works. Section V concludes the paper.

2. PROPOSED FRAMEWORK

Our primary objective is to empower a solitary district at once testing of an outline by using any given arrangement of test examples. Upon the finish of the stacking of an example into the output cells, dispatch and catch operations will be carried out in every locale,

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each one in turn, bringing about the same number of sets of dispatch and catch beats as the quantity of districts. An example may dispatch transition(s) from an arrangement of flip-lemon which might perhaps compass various districts and catch these moves in the region(s) being tested. The test is that any test example may be testing any arrangement of locales by dispatching moves from whatever other arrangement of districts.

Testing one locale at once in at-rate testing obliges dispatching and catching moves inside one district at once, conveying funds in dispatch and catch power. While in static testing catch stunning inverse toward information stream has been demonstrated to consider the utilization of test examples in place, in segment based at-pace testing the dispatch operation forces extra requirements and requires further DFT support.

Power reserve funds amid dispatch and catch in LOS and LOC testing by means of apportioning can be achieved while having the capacity to apply the examples of a force unconscious ATPG instrument if:

1) acyclically formed locales are tested in a request inverse to the information stream;

2) Region interface registers can be restored back to their heap state upon dispatch and catch.

The second point above contrasts between the LOS- and LOC-based testing, accordingly obliging diverse DFT bolsters in the two plans.

2.1 DFT Support and Implementation for LOC Testing

To restore the heap state (the bit moved) of the interface (utilitarian) register upon the dispatch and catch operations, one shadow (test) register is implanted for each interface register. All thought the movement operations, the shadow register duplicate the substance of the interface register, and amid the catch window, the shadow register is not timed, guaranteeing that the replicated esteem the last move cycle is held. Upon every dispatch and catch operation that the interface register gets include in, its heap state is restored by replicating the substance of the shadow enlist over into the interface register.

Fig. 1 gives the DfT backing to the heap state restore system. Successfully, a multiplexer and a shadow flip-lemon is embedded for the interface register, multiplying the measure of the interface sweep cell. The recently embedded rationale falls on the test ways just, causing to timing punishment at all. The restore sign can be effortlessly created on-chip as indicated in the same figure. The total cost is N_{int} MUXes and N_{int} + 2 flip-flops for N_{int} interface registers.

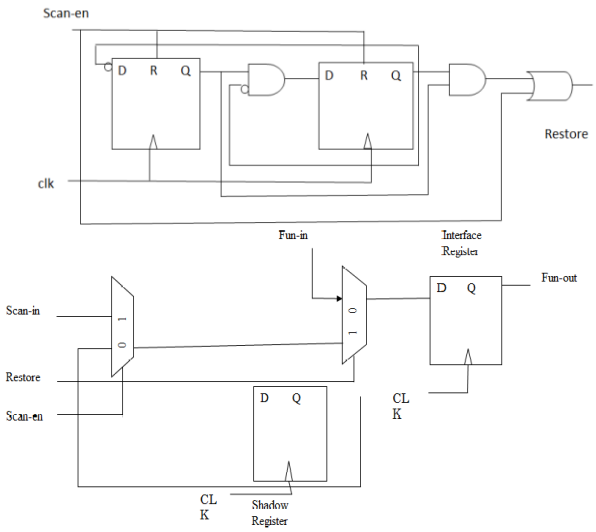

Fig. 1. DFT support for restore operations in LOC testing

2.2 DFT Support and Implementation for LOS Testing

As the LOS scheme launches transitions via a shift operation, a set of test patterns is valid as long as the final scan cell ordering in the chain perfectly matches that during test generation. Therefore, LOS pattern generation should be done subsequent to scan stitching in conventional LOS.

The only additional constraint imposed on scan stitching by the proposed partitioning scheme is that the interface registers of each region should be placed in consecutive positions on the scan chain and that they must be stitched in a bidirectional manner. Such a special stitching and the associated DfT support are required only for the interface registers in order to enable a proper rewind operation; minimization of the number of interface registers helps to minimize the area cost incurred. Finally, restoring the value of the rightmost bit of a group of interface registers subsequent to the launch operation necessitates an extra flip-flop, which holds the value of the rightmost interface bit upon launch; a subsequent rewind

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operation restores the value of the rightmost interface register from the value in this extra flip-flop.

Bidirectional stitching of the interface registers in a region requires one additional multiplexer for each interface register; this multiplexer can be inserted on the scan path (on the 1-input of the scan multiplexer), imposing no impact on the functional timing of the design whatsoever. The proposed scan architecture that supports design partitioning into two regions is provided in Fig. 2, also illustrating the simple and cost-effective on-chip generation of the rewind signal out of the scan-enable and clock signals. The total cost is N_{int} MUXes and R_{int} + 1 flip-flops for N_{int} interface registers and R_{int} regions, which have at least one interface register.

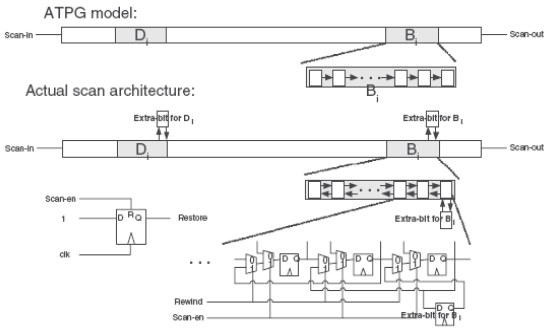

Fig. 2.ATPG model and actual scan architecture for low-power LOS testing

2.3 DFT Support and Implementation for Mixed Testing

As the LOS and LOC testing may uniquely detect faults in a mutually exclusive manner, a mixed test with both LOS and LOC patterns typically yields a higher fault coverage level compared to either testing scheme applied alone. In this section, we outline the DfT support required to support low-power mixed testing with both LOS and LOC patterns.

While the bidirectional stitching of interface registers fails to enable the proposed low-power LOC testing, the shadow register support can be utilized to enable the proposed low-power LOS testing; the shadow registers can replace the bidirectional stitching for the restoration of the load state in LOS testing. Therefore, to support both low-power LOS and LOC testing, the architecture in Fig. 1 can be utilized, but with a couple of changes; the shadow registers should be clocked only during the shift cycles, and a unified Restore signal should be generated to support both LOS and LOC operations. The simple circuitry that generates this unified Restore signal is provided in Fig. 3. The LOS/LOC signal, which denotes the type of test for the current pat tern being applied and can be controlled by a programmable register bit (no need for an additional pin), can make the selection of the proper signal.

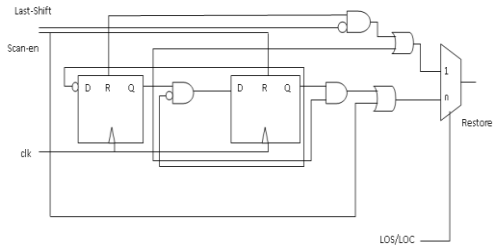

Fig. 3. Unified restore signal for mixed testing with LOC and LOS patterns

2.4 Block Logic Method for prevents redundant switching in combinational circuits

Inserting blocking logic into the stimulus path of the scan flip-flops [as shown in Fig.4(a)] to prevent propagation of scan-ripple effect to logic gates offers a simple and effective solution to significantly reduce test power, independent of test set. Blocking gates (of type NOR or NAND) are controlled by the test enable signal [as in Fig. 4(b)],and the stimulus paths remain fixed at either logic "0" or "1" during the entire scan shift operation.

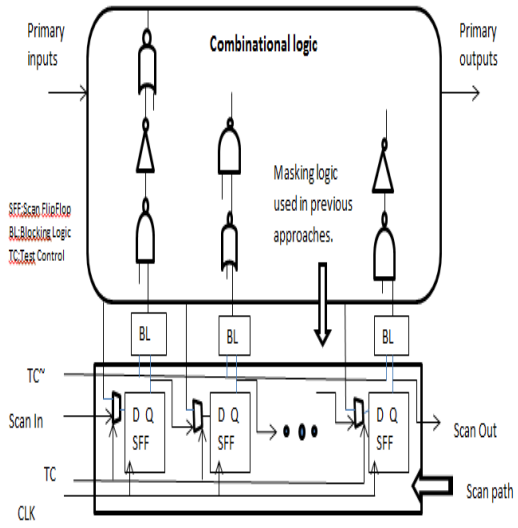

Fig. 4(a).Scan architecture with blocking circuitry

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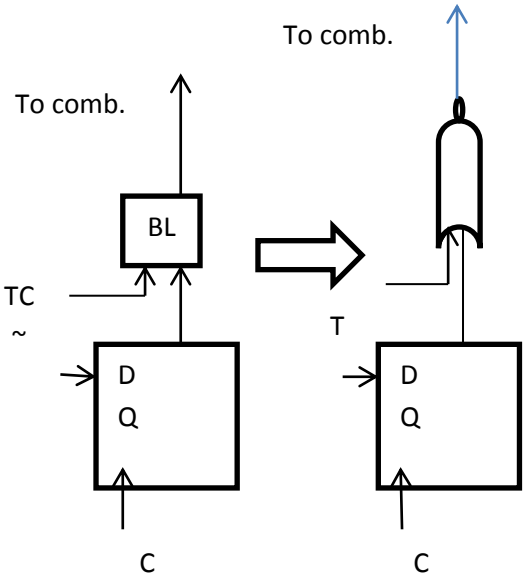

Fig. 4(b). Blocking Logic

2.5 Selective trigger scan architecture for reduce transition between test vectors

We start explanation of our proposed architecture with a simple example. Let us assume that V_1 in Fig.5a is an existing test vector in a scan chain and V_2 is the next test vector that must be shifted. Comparing V_1 and V_2 transitions (Fig.5a), there are only three differences in their bits that are called necessary transitions. If we were to use a standard scan chain and shift V_2 into the scan chain in eight test clocks, with each shift, transitions shown in Fig.5b would occur. For example, shifting the rightmost 1 of V_2 into the scan chain causes five transitions in the eight scan flip-flops. Altogether, shifting V_2 would cause 32 transitions that are called unnecessary transitions. On the other hand, parallel loading V_2 directly into our architecture eliminates unnecessary transitions on the input of a CUT.

Hence, our scan architecture should eliminate the unnecessary transitions. In addition, the following features should be considered for the proposed scan architecture and DFT method:

- Scan architecture should not add extra inputs compared to a conventional scan approach.
- A DFT approach must add no delay to the normal operation of the circuit.

The proposed architecture, shown in Fig. 6, serves two purposes. One is to reduce the activity at the data outputs and the second is to facilitate test data compression. As shown in Fig. 6, the NOR gate compare the previous cell and next cell test vector, if the value will be same again the previous value saved into the TR. If the value will be differ the next cell value saved into TR.

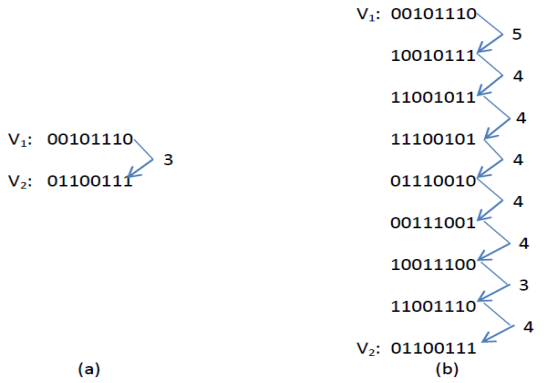

Fig. 5. (a). Transitions between 2 test vectors. (b). Unnecessary transitions in scan architecture

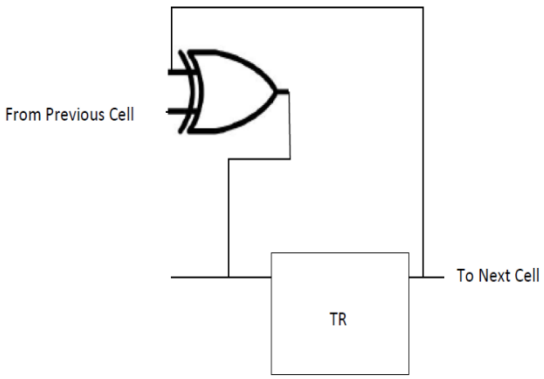

Fig. 6. Scan cell structure of the proposed architecture

3. EXPERIMENTAL RESULTS

We evaluate our design using modelsim. We simulate an ISCAS89 benchmark circuits and obtained power, area and time. We choose block logic, mixed at-speed testing and selective trigger for experimental evaluation. Fig.7. Represents, the simulation result of block logic, mixed-at-speed testing and selective trigger. Selective trigger reduced number of transition between test vectors. Block logic prevents redundant data transition into combinational circuits.. Fig. 8. Shows the power report of block logic, mixed-at-speed testing and selective trigger. The total power consumption is 131 MHz. The flip-flop count is reduced. So, the area

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overhead is reduced. Table. 1. Shows the static power and area comparison.

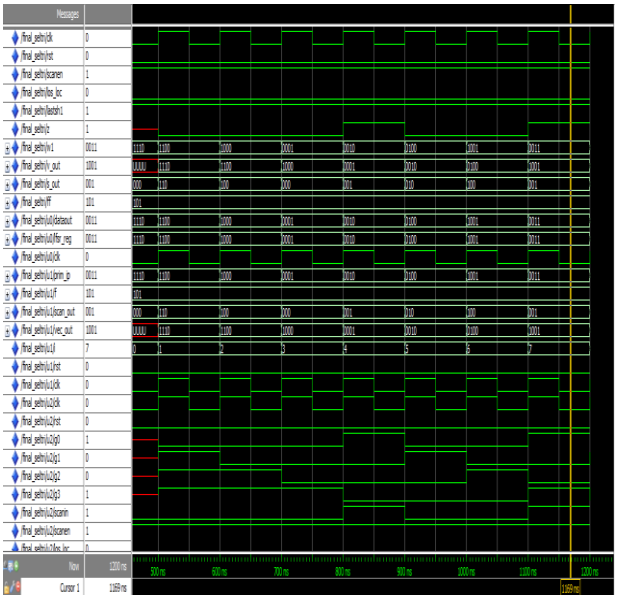
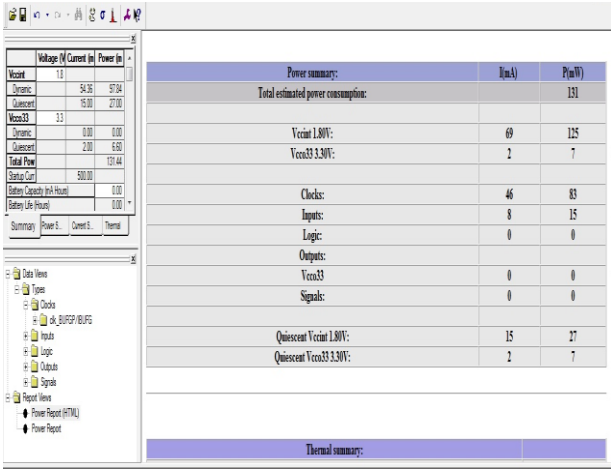


Fig.7. The simulation result of proposed architecture



Power summary:	I(mA)	P(mW)
Total estimated power consumption:		131
Vccint 1.80V:	69	125
Vcco33 3.30V:	2	7
Clocks:	46	83
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Fig. 8. Power report for proposed architecture

Table.1. Power and Area comparison analysis

Circuit	Power report (MHz)	Gate count
S27 circuit without DFT	152	207
S27 circuit with DFT	131	142

4. RELATED WORK

Sweep cell testing has been widely used to build shortcoming scope in the CUT. The proposed outline dividing strategy that can decrease power dissemination amid dispatch and catch operations in at-velocity testing. Square rationale anticipates repetitive information move into combinational circuits. Specific trigger diminishes number moves between sweep cells and test vectors. So, the power consumption in the scan cell testing have been reduced.

5. CONCLUSION

In this paper, block logic, mixed-at-speed testing and a selective trigger are proposed for power minimization. At shifting operation redundant data transferred into the combinational circuit. At run time, enable the block logic to block data up to finishing the shifting operation. Selective trigger neither reduces the number transitions between test vectors to using NOR gate. Both of these methods, used to minimize the power and area compared to the existing method. Thereafter, the static power is reduced by 6.1% to 11% and the area overhead reduced by 47% compared to Mixed At-Speed testing with slight increment in dynamic power.

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