EMERGING FET TECHNOLOGIES

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ABSTRACT
This paper discusses the upcoming FET technologies to maintain the constant pace of progress in ultra-dense integrated electronic circuitry. The emerging alternatives: Carbon Nanotube Field Effect Transistor (CNFET), Tunnel Field Effect Transistor (TFET), Single electron transistor (SET), Quantum dots, Organic Field Effect Transistors (OFET) and Nanowire Transistors are discussed. The review seeks to provoke keen interest in these futuristic nanotechnologies.

Keywords
Nanotechnology, Carbon nanotubes, Single electron transistor, Quantum dot, Tunnel FET, Organic FET, Nanowire transistor.

1. INTRODUCTION

In the past few years, the dimensions of MOSFET have decreased dramatically. Few prototype FETs with gate length in nanometer scale have been successfully fabricated, which exhibit excellent electrical characteristics. The advancement in MOSFET technology has followed Moore's law whereby number of transistors incorporated on a chip doubles every 18 months, thereby gaining speed and density. With decreasing oxide thickness below 1.5nm in short length MOSFET devices causes gate oxide leakage. The obvious remedy is to replace silicon dioxide with an insulator that has significantly higher dielectric constant than 3.9 which allows the device to operate using the same capacitance, but with a higher physical thickness that suppresses direct current leakage, and hence, lower power consumption [10]. Though, shrinking the conventional MOSFET beyond the nanometer technology requires innovations to circumvent barriers due to fundamental physics. This pace of MOSFET technology scaling has accelerated the introduction to alternative technologies which would enable continued improvements in the density and performance. These new devices whose dimensions are on the scale of tens of nanometers are called *nano-devices* and their science is termed as *nano-technology.*

Nanotechnology is the science of building materials and devices on the nanometer length scale (at the level of atoms , molecules and supramolecular structures). The control of matter at this scale means conforming the fundamental properties exactly at the scale where they are determined. Such a structure has at least one dimension measured in nanometers [1].

2. PROMISING FET TECHNOLOGIES

The conventional MOSFETs operate via the movement of masses of electrons in bulk matter. Instead, the new technological devices adopt the quantum mechanical phenomena that emerge at the nanometer geometries, where the discrete nature of electrons cannot be ignored. Recent research, however, has brought new devices into picture as mentioned below:

- Carbon nanotube field effect transistors
- Tunnel field effect transistors
- Single electron transistor
- Quantum dots
- Organic field effect transistors
- Nanowire transistors

In this paper, the advantages/drawbacks, the operation principles and the challenges for commercialization of present and promising nanotechnology devices are investigated.

3. CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNFET)

A carbon nanotube device is similar to a MOSFET where gate controls the flow of current by varying field through a channel. The innovation here is the channel which is the tiny tubular structure known as *carbon nanotube*. CNTs are graphene, which is a two-dimensional honeycomb lattice of carbon atoms, sheets

rolled up into cylinders. They show either metallic or semiconducting properties depending on the direction how CNT are rolled up (chirality).
Its structure shown in Figure 1 have remarkable material properties, such as large current carrying capacity, the excellent mechanical and thermal stability, and high thermal conductivity. High-k dielectrics can be easily incorporated in CNTFETs due to the absence of dangling bonds. Also, since both NMOS and PMOS transistors show almost identical I-V characteristics, it becomes a significant advantage for CMOS circuit design. Furthermore, they are very attractive to Si-based semiconductor industry for the following reasons: 1) CNFETs show improvement in device performance such as low power and high speed 2) their operating principles and devices structure are similar to Si-based CMOS transistors; therefore, the CMOS design infrastructure could be reused [1].

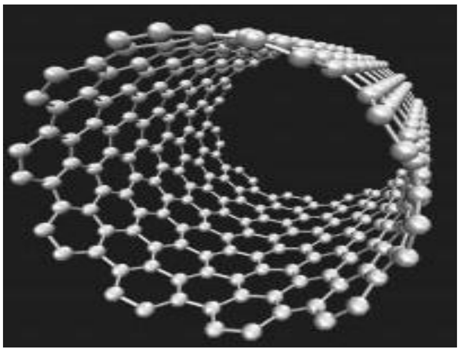

Figure 1: A single walled carbon nanotube [4]

Even though CNT-based electronics presents great promise, there are several difficult challenges to be solved [4].

- Further scaling is a problem.
- Multi level interconnects, such as different metal layers are still unavailable with carbon nanotubes.
- New fabrication technology is not at production level.

4. TUNNEL FIELD EFFECT TRANSISTORS (TFET)

Tunnel field-effect transistors (TFETs) use electric-field control of band-to-band tunneling as the current gating mechanism. These transistors have emerged as leading contenders to outperform CMOS at low voltages. This stems from the ability of the TFET to achieve a subthreshold swing (*SS*) of less than 60 mV/decade at room temperature. Lower subthreshold swing enables a reduction in voltage supply and a path to reduce the power consumption of electronic devices. This enables TFET to switch on and off at lower voltages as compared to MOSFETs [8].
The major drawback is low on-state drain current. The increased device sensitivity to radiation, noise and process variation at reduced VDD poses further challenge on robust circuit operation using TFETs. Lots of experimental work is been done on Tunnel FET to boost the ON state Drain Current.

5. SINGLE ELECTRON TRANSISTORS (SET)

SETs are very attractive devices due to their small size and low-power dissipation at good speed. The basic structure of SET consists of three-terminals such as drain, gate, source, and the second gate is an optional. A schematic of SET, as shown in Figure 2, is analogous to that of conventional MOSFETs.

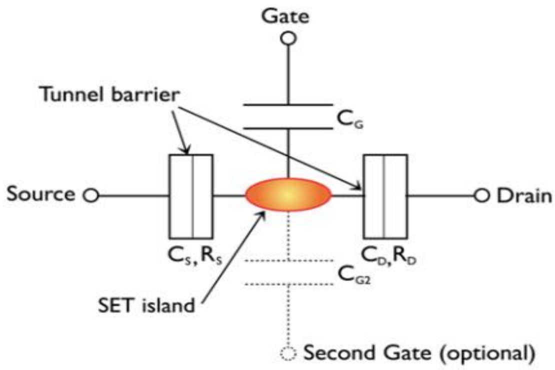

Figure 2: Schematic of basic Single electron transistor [2]

However, SET has a tiny conductive island coupled to a gate electrode with gate capacitance C_G. Source and drain electrodes are connected to the island through a tunnel barrier (junction). The tunnel barrier, which controls the motion of every single electron, consists of two conductors separated by thin layer and it is modeled as tunneling resistances $R_{D,S}$ and junction capacitances $C_{D,S}$. The increased gate bias attracts electrons to the island only through either drain or source tunnel barrier, and the number of electrons in the island only has a fixed integer. If we make the second tunnel junction barrier higher than the first barrier, then certain number of electrons will have to be accumulated on the island before any electron can tunnel through to the drain. This phenomenon of blocking an electron from immediately leaving the island is called Coulomb blockade. Therefore, the increased gate bias makes electrons flow one by one when a small voltage is applied between the source and drain electrodes by means of the “Coulomb blockade” phenomenon [2], [4], [5].

Easy scalability due to atomic level operation, low power dissipation because of small number of electrons to accomplish basic operation and high operating speed due to involvement of transference of small number of electrons make SETs attractive. The major drawbacks are poor current drive capability as compared to CMOS devices and the need for low-temperature operation [1]. The operation of SET circuits can be upset by the presence of one single stray charge and hence they are not likely to be used for large CMOS type applications but are quite useful for designing memories.

6. QUANTUM DOTS

For logic operation we do not need the actual flow of electrons. We need an efficient encoding system that transfers the state of a dot through an array of devices. This is where the quantum dots come into the picture. Quantum dots are devices with tunnel junctions in all three dimensions of the island. Thus, we have an electron box, which the excess electron is confined to. This excess electron determines the state of the system and when these dots are arranged in cells it is possible to design logic circuits that can function efficiently. The advantage of Quantum Cell array (QCA) lies in the extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power-delay product.

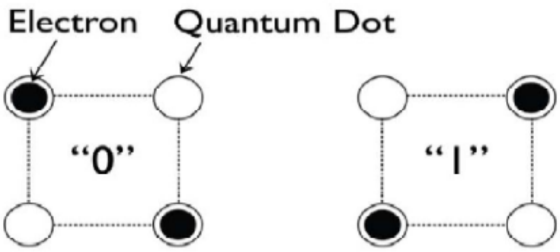

Figure 3: Four Dot QCA Cells [6]

A basic QCA cell consists of four quantum dots located at the corners of a square, coupled by tunnel barriers. If the cell is biased so that there are two excess electrons among the four dots, Coulomb repulsion will force the electrons to opposite corners. There are thus two energetically equivalent polarizations, as shown in Figure 3. These two polarizations can be labeled logic ‘0’ and ‘1’, and, by properly arranging cells so that the polarization of one cell sets the polarization of a nearby cell, it is possible to implement all combinational logic functions. A tremendous advantage of QCA devices is the simplified interconnect which is possible with this paradigm [6]. Since the cells communicate only with their nearest neighbours, there is no need for long interconnect lines. The inputs are applied to the cells at the edge of the system and the computation proceeds until the output appears at cells at the edge of the QCA array.

We try to communicate information not by transmitting current but just by transmitting the state of the device. This eliminates many problems faced by the switching devices and hence the quantum dots appear to have a bright future. These devices can be used to construct logic gates and quantum wires and effectively functioning logic circuits. Despite of obstacles like background charge, sensitivity to input voltage fluctuations; the quantum devices hold promise and researchers are relentless in making integrated circuits with these devices.

7. ORGANIC FIELD EFFECT TRANSISTORS (OFET)

OFETs are composed of three terminals, the source, drain, and gate, as well as a semiconductor layer and an insulating layer between the semiconductor and gate as shown in Figure 4. The insulator can be made of a variety of dielectric materials, though SiO2 is a common choice. A voltage is applied to the gate to control the amount of current flow between the source and drain.

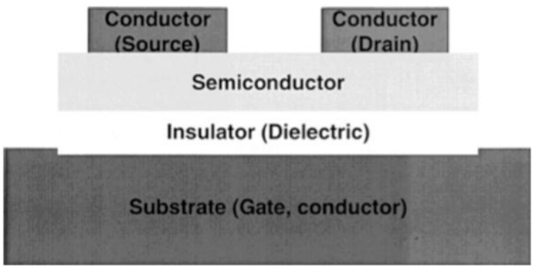

Figure 4: Typical structure of an Organic Field Effect Transistor [7]

OFET research generally seeks to optimize two important values, the carrier mobility and the on/off current ratio. Carrier mobility is directly proportional to semiconductor conductivity, and is thus directly related to the performance of the device. The on/off current ratio is the ratio of the saturation current when VGS is high to the leakage current when VGS is zero. Increasing this ratio is important in the switch-like behavior of OFETs [7].

OFET research over recent decades has lead to very promising p-type devices based on a wide selection of OSCs. Problems relating to electron mobility, chemical deposition techniques still limit OFETs. However, if these obstacles are overcome, OFETs could be used to create cost-effective, flexible, lightweight, and environmentally-friendly circuits.

8. NANOWIRE (NW) TRANSISTORS

Nanowire field-effect transistors (NWFETs) or gate-all around FETs with a thin nanowire channel are promising candidates since their non-planar geometry provides superior electrostatic control of the channel than the conventional planar structures. The increasing attention in nanowire research emerges from several key aspects: cost-effective fabrication which prevents some fabrication challenges, higher carrier mobility by means of the reduction of scattering resulting from the crystalline structure, smooth surfaces and the ability to produce radial and axial nanowire heterostructures, better scalability resulting from the fact that diameter of nanowires can be controlled down to well below 10 nm [3]. Nanowire surrounding gate transistors are promising candidates for the next generation high-speed analog and VLSI technologies. This low power device can be used to develop future high speed memories and integrated circuits to enable wireless communications [9].

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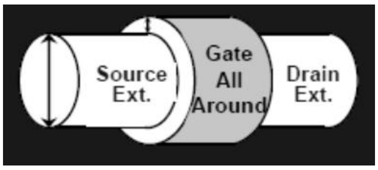

Figure 5: Silicon Nanowire Device Structure [9]

However, due to their smaller nanowire diameters, the inversion charge changes from surface inversion to bulk inversion due to quantum confinement which degrades the charge transport. Also, variations in nanowire diameters may lead to a variation in FET threshold voltage. Reducing variability is therefore a key challenge in making nanowire FETs a possible working technology.

9. CONCLUSIONS

As the feature size of component reaches to its fundamental limits, various types of researches are carried out for fulfilling the next century technology demands. It will give birth to new type of devices that promises advantages of reduction of size, low power dissipation, high noise immunity, faster and better logic swing, high gain and least possible feature size. The future is near when the Gordon Moore's law is satisfactorily achieved by advancement of nanoelectronics. With the advanced research work in the field of nanoelectronics and its allied fields, the coming future hold the hands of nanoscience for better pleased future of technology. Nanocomputers will only be possible after breakthroughs on many fronts. It remains uncertain which discipline would provide the earliest breakthrough. However, once they arrive, they will change the face of electronic computing and our technological infrastructure.

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