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EMERGING MEMORY TECHNOLOGIES

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ABSTRACT
For almost last three years computer memory system use volatile, high speed memory technology like SRAM for cache, DRAM for main memory, flash memory for low power consumption applications. The fast access to memory is the major bottleneck for CPU performance. The emerging memory technology could improve the performance of CPU. The focus of this paper is to summarize the emerging technology of memory system design, presents these new memory technologies and survey the recent trends for memory technologies to advance memory hierarchies.

Keywords
Column access strobe; Row access strobe; Floating gate; joint electron device engineering council; magnetic tunnel junction.

1. INTRODUCTION
In the history of technology, emerging memory technologies are current advances and innovation in memory field of technology. CMOS memories basically divided into two parts i.e SRAM and DRAM. Technology scaling of SRAM and DRAM are increasingly constrained by fundamental technology limits. In particular, the increasing leakage power for SRAM and the increasing refresh dynamic power for DRAM have posed challenges to circuit and architectural design for future memory hierarchy.

Non volatile memory market share has been continuously growing in the past few years, and further growth in the near future is foreseen, especially for Flash memories due to their enhanced flexibility against electrically programmable read-only memories [1]. The complexity of logic functions and architectures inside a Flash memory device has grown in order to face the need for more complex system interfaces and to manage the increased amount of stored data.
Non volatile memories (NVM's) will account for 12% of the total available market, and Flash memory cells are forecast to be more than 50% of the year 2000 NVM market.[2] The nano memories are very promising memory technology for traditional CMOS memory. The main advantage of MRAM is minimum static power dissipation. The magnetic tunnel junction is the one of the interested candidates of MRAM as identified by IRTS.[8]

2.PROMISING MEMORY TECHNOLOGIES
The conventional SRAM cell requires large power consumption and DRAM is asynchronously control the read/write access of rows and columns. The DRAM cell requires dynamic refresh circuits. The industry is always looking for ways to decrease power consumption, increase density and develop different architectures. Recent research however has brought new memory devices into picture as mentioned below.

- Synchronous Dynamic RAM
- Flash memory
- Spin orbit torque MRAM
- Nano memory device

In this paper the operation principle, advantages and drawback of different memory technologies are investigated.

2. SYNCHRONOUS DYNAMIC RAM (SDRAM)
SDRAM devices were defined by JEDEC to address the performance limitations of older DRAM architectures. Currently SDRAM synchronise with the clock of 66-100M_Z. The burst access time of SDRAM is faster than conventional DRAM as SDRAM adopted the technology such as pipeline which is not available with conventional DRAM[5]. Some operational features of the SDRAM, which are not available in conventional DRAMs, are: synchronous control logic, controls with

commands, multiple bank architecture, refresh mode, memory I/O power supplies, selectable CAS latency, selectable burst length and mode register which is shown in figure 1.

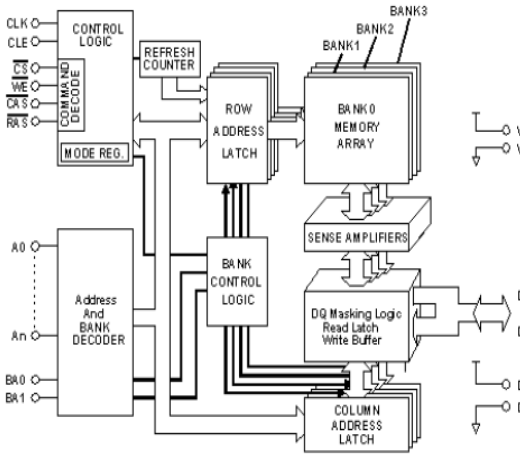

Fig.1 Block diagram of SDRAM [5]

4. Flash memory

The flash memories are non volatile memories. Flash memories based on the concept of floating gate MOSFET.The flash memories are divided into NAND and NOR flash memories depending on the structure for the interconnection between memory calls. In NAND device cells are connected in series and in NOR connected in parallel. In flash memories, hot electron injection and fowler-nordheim tunnelling mechanism is used to write data in memory cell and to read data comparator and sense amplifier circuit is used.

4.1 HOT ELECTRON INJECTION

Hot carrier injection phenomena usually refer in MOSETs where a carrier is injected from the conducting channel in the silicon substrate to the gate dielectric.

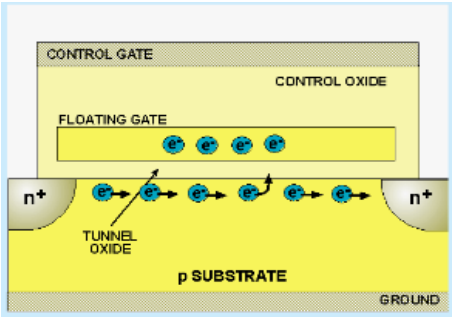

Fig. 2 Electron injection into floating gate

In order for injection occurs, two conditions required, a high current flowing through the transistor's channel and a high gate-to-drain electric field. When channel to drain electric field is high, electrons expelled with enough kinetic energy and scattered upward into the gate oxide, overcome the potential difference in electron affinities between the Si and SiO2, inject into the oxide conduction band, and be collected by the floating gate.

4.2 FOWLER-NORDHEIM TUNNELING

The Fowler-Nordheim tunnelling is a quantum mechanical tunnelling mechanism induced by the electric field as shown in figure 3. Applying a strong electric field across the thin oxide, it is possible to force a large electron tunnelling current through it without destroying its dielectric properties.

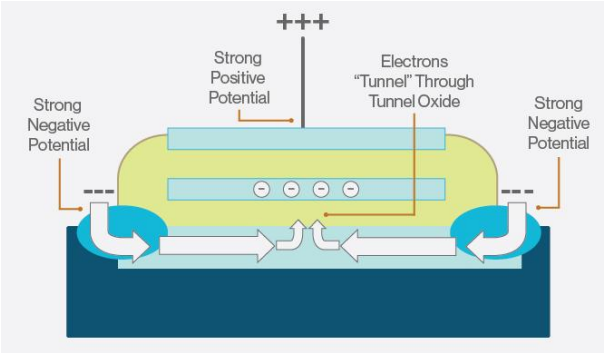

Fig.3 Fowler-Nordheim Tunnelling

5.SPIN ORBIT TORQUE MRAM

The magnetic RAM is a non volatile memory which is based on a magnetic tunnel junction storage device[6]. Among NRAM technology Spin orbit torque RAM gains attention as it is non volatile, it improves the read stability and write current is much lower.

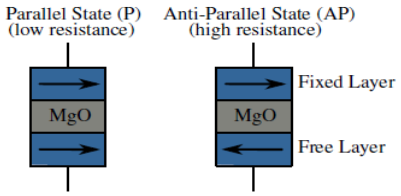

Fig.4 MTJ resistance according to the magnetization of the free layer [7]

Spin orbit torque NRAM based on MTJ cell in which data is stored in the form of resistance state value. It consists of two ferromagnetic material separated by MgO. In MTJ device one material consider as fixed layer or reference layer while other material as a free layer. When the direction of the magnetic field of the free layer is parallel to the fixed layer, the MTJ has a low resistance state. When the direction of the magnetic field of free layer is anti-parallel to the fixed layer, The MTJ has a high resistance state. This high and low resistance values are used to represent logic '1' and '0' values respectively. The SOT MRAM bit-cell has an

additional terminal to separate the (unidirectional) read and the (bidirectional) write path which are perpendicular to each other as shown in figure 5.
The terminals comprise a read line, a write line, a source line and a word line. The word line is used to access the required bit-cell during memory accesses via the NMOS-based access transistor[7].

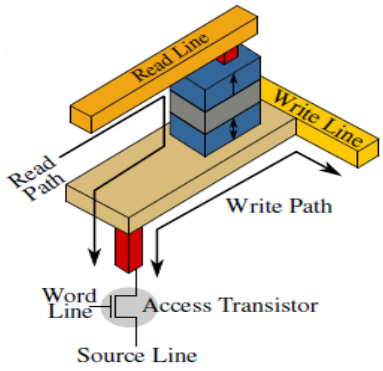

Fig.5 SOT memory[7]

6. NANO MEMORY DEVICE

The nanomemory device works on the nanomechanical principal rather than change the properties of material. The nanomemory device used the carbon nanotube for the bit cells. The nano memory devices are faster, scalable and dense than DRAM[10]. The nano memory device consists of two parts ,the capsule which holds the smaller charged shuttle. The capsule is nanotube and shuttle is a buckyball. The state of the memory device is determined by the location of the shuttle: if it is on one side of the capsule, we treat it as a '1'; on the other we treat it as a '0'. The Van der Waals forces between the tube and the shuttle will tightly bind the shuttle to one end of the tube or the other. There is an unstable equilibrium point when the shuttle is in the exact middle of the capsule, but our proposed scheme for writing to the device would prevent the shuttle from ever coming to rest there.

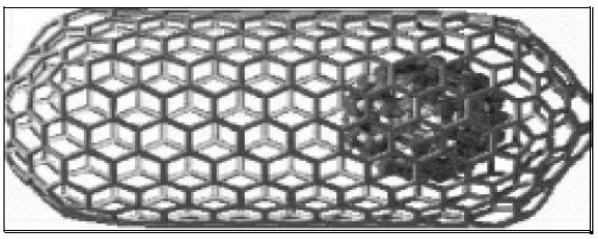

Fig. 6 Nanomemory Device[10]

The potential energy of the shuttle at various locations in the NMD shown in figure. The solid line indicates the potential energy curve when no electric field is applied. Notice that the two potential energy wells are found when the shuttle is on one side of the capsule or the other. These wells keep the shuttle bound to either side of the capsule. The other two lines display the potential energy when a two-volt potential difference is applied.

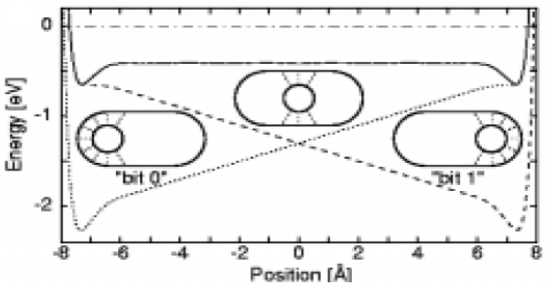

Fig.7 Potential energy of the shuttle at different locations in the capsule [10]

When such a voltage is applied, there exists only one local minimum, and the shuttle will move to that side of the tube. It is with this two-volt potential difference that we can write to the NMD. In general the amount of voltage which needs to be applied depends upon the length of the capsule. To read the nanomemory devices the state of the device must have to be sensed.

7. CONCLUSION

As the power dissipation is the main constraint for basic memory devices, various types of research are carried out for gratifying the next century technology demands. It will give birth to new type of devices that promises advantages of low power dissipation, small size device and high read/write access of memory cell. This paper reviewed recent development for memory technology. With the advanced research work in the field of nanoelectronics, the upcoming future hold the hands of nanoscience for better pleased future of memory technology.

8. ACKNOWLEDGMENTS

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